7 nm and the Dawn of Low-power, High-Performance Computing

Synopsys

ABSTRACT

In this session, senior R&D from Synopsys will discuss the numerous metallurgy- and lithography-specific challenges associated with the 7 nm process node and how these call for innovative and collaborative solutions throughout the design-implementation flow. They will outline how interconnect management has become a primary focus thus becoming a key component for the enablement of ultra-high-performance compute devices. With exponentially increasing line resistivity, borne of interconnects nearing the atomic scale, they will share how design optimality demands a hyper-converged solution spanning the breadth of physical synthesis and physical implementation. With shared technologies and flows including congestion-aware wire and via estimation, extended-stack-high-R-aware layer-optimization, advanced, non-default rule application and enhanced-via-topology modeling and insertion, they will discuss the combined solution of DC Graphical and IC Compiler II and the industry-leading results this converged design-flow delivers. They will further demonstrate how by delivering leading correlation between front-end and back-end, mutual customers are aided in maintaining project schedules and ultimately in realizing best-in-class and first-to-market solutions.

Synopsys will additionally share how another key concern for high-performance, low-power compute enablement is the availability of high-quality and optimum-delay clocking implementations. Specifically, how the need to address the challenges of manufacturing-and-lithography-induced variation, growing load-capacitances and the aforementioned interconnect-delay increases, necessitates that any final clocking topology be tuned to meet numerous, competing demands. In particular, meeting the competing goals of on-chip-variation (OCV) robustness, dynamic power reduction and latency minimization while concurrently addressing signal integrity, reliability and cost factors. Synopsys will share some of the latest clocking technologies available in IC Compiler II that seamlessly blends ease-of-use with highly differentiated and disruptive out-of-the-box results. This includes robust, pico-second-accurate mesh topologies, lower-power multi-source structures and other, highly optimized configurations. Coupled with the full-flow interconnect and enhanced-via-topology optimization technologies outlined above, these leading clocking solutions help deliver a significant frequency uplift while maintaining or even reducing the total power envelope.

Key to all of these advancements for low-power, high-performance computing is the shared experience of an ongoing, extensive and deep collaboration effort. Synopsys will discuss how the OIP program ultimately accelerates customer access to the latest nodes and is paramount in the delivery of a qualified flow that spans the entire Galaxy platform.

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Silicon to Software™

7 nm and the Dawn of Low-power, High-Performance Computing

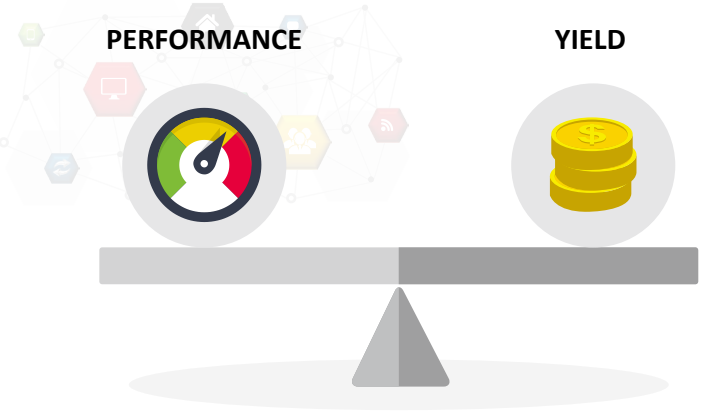
Converged enablement for next-generation SoCs targeting big data and networking infrastructure utilizing DC Graphical and IC Compiler II

Dr. Henry Sheng, Director R&D, Design Group

September 22nd 2016

N7: For SoCs Everywhere

Optimal Power, Performance and Area with Joint Reference Flow



PROCESS + REFERENCE FLOW + IMPLEMENTATION

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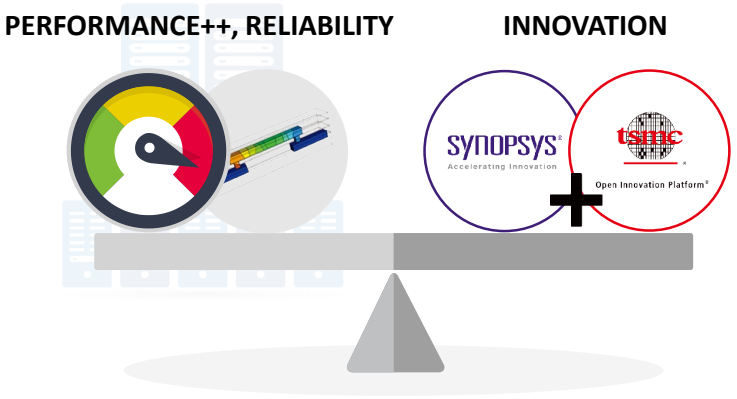
N7 HPC: A Collaborative Enterprise



Reducing Cost of Ownership Through Collaborative Innovation

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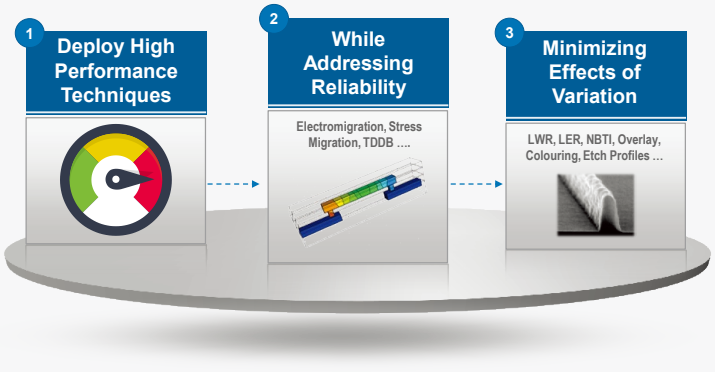
Synopsys: Proven Path to HPC Design

Collaborative Pathfinding and Solution Delivery for TSMC N7



Requires Solutions Throughout the Design Implementation Flow

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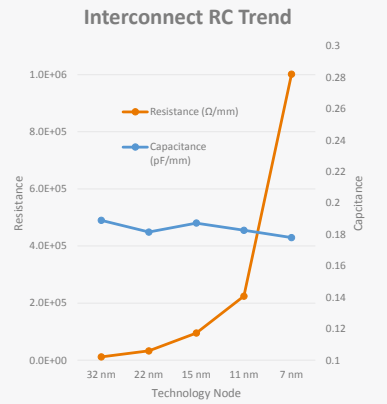
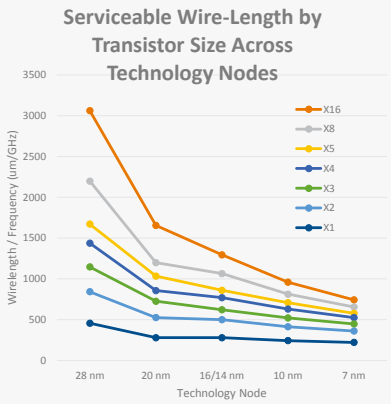
Interconnect: The Primary Challenge

Node-Scaling-Related High Performance Trends





Interface-Layer Effects and Grain Scattering Impacting Resistance Scaling

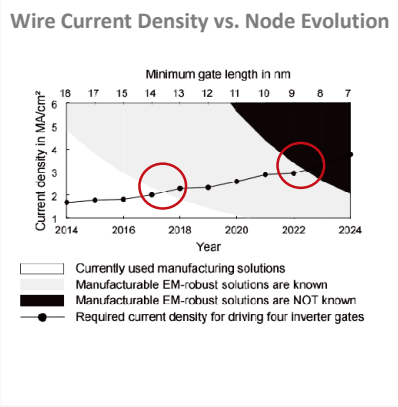
Flight-Time Increasing Diminishing Benefit from Device Sizing

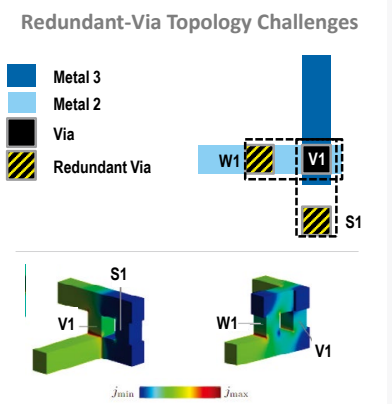
Source: Serkan Kincal, et al., "RC Performance Evaluation of Interconnect Architecture Options Beyond the 10 -nm Logic Node," IEEE (2014)

Source: Greg Yeric, "Moore's Law at 50: Are we planning for retirement?", IEEE (2015)

Electromigration and Stress Migration

Reducing Wire Cross-Sections, Increasing Current Densities





HPC Accelerates Time and Current Density "Up-and-to-the-right"

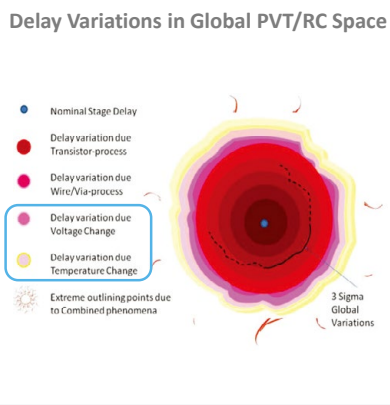
Via Position and Selection is Paramount to Minimizing Current Density

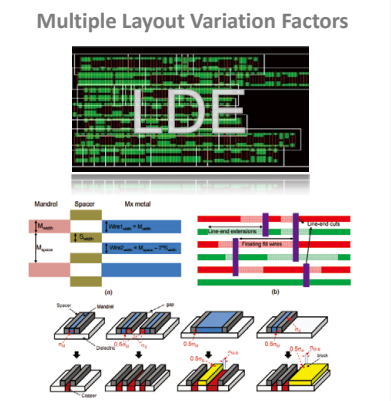
Source: Jens Lienig, Electromigration and Its Impact on Physical Design in Future Technologies, ISPD 2013

Source: Jens Lienig et. al., Load-aware redundant-via insertion for electromigration avoidance

Design Variation and 2nd Order Effects

Increasing Inter/Intra-Die Variations Demand Holistic Solutions





Increasing Parasitic Variability Requires Robust Design/Analysis Methodologies

Variation Mitigation for Known Design Effects. Effective Analysis

Source: Alexander Tetelbaum, Corner-based Timing Signoff and What Is Next, 2014

Source: Andrew Khang, "New Game, New Goal Posts: A Recent History of Timing Closure"

Meeting the Challenges of HPC

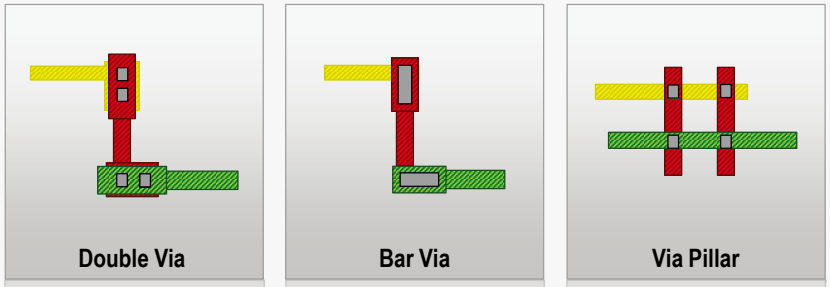
Leveraging a Proven Path to HPC Design

PERFORMANCE	RELIABILITY	VARIATION
Performance-Driven Via-Topology Selection and De-Selection	Automated, Optimized Via Insertion	Full-Flow MCMM Support
Critical-Net Layer Promotion	User-Driven, Via/Wire Topology Choices	OCV/AOCV/POCV (LVF)-Driven Optimization
Criticality-and-Density-Aware Demotion	Sign-off Correlated EM/IR Analysis	Variation-Driven Clock-Topology Implementation

Seamless Deployment Throughout the Implementation Flow

Via Pillars for Manufacturability

Traditional Redundant Vias No Longer Applicable at N7



- Via pillars as an alternative to traditional RVI
  - Double via and bar via both violate lithography rules for N7
  - More route/congestion intensive, but meet lithography requirements

50% Resistance Reduction – Single vs. 2x1 Via Pillar

Via Pillars for Performance and Reliability

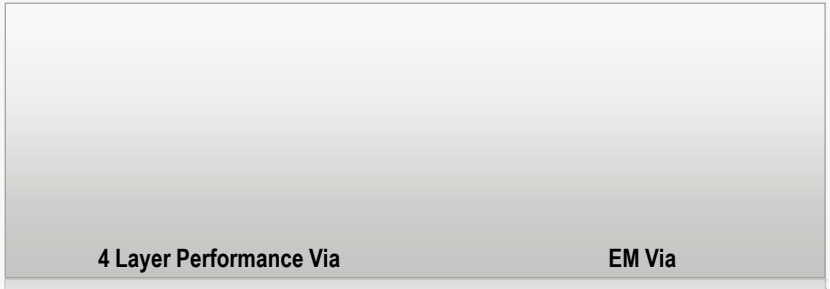
Addressing HPC Challenges Through Flow Enhancements

- Significant **resistance reduction** on multi-patterned layers
- **Electromigration friendly** structures improves **resilience** for prolonged, high performance operation

Need Dynamic Via-Pillar Solution to Meet Patterning Demands

Multiple Via-Pillar Styles for Flexibility

Automatic Via-Pillar Creation Streamlines Flow

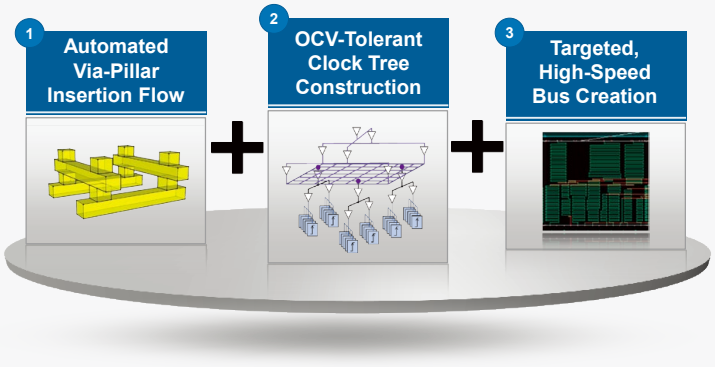


- Each category may have various configurations and possibilities
- Aggressive and route intensive, vs. less aggressive and route friendly

Full-Flow Modeling and Implementation Delivers Convergence

Synopsys' N7 HPC Design Flow

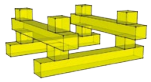
Full-Flow Solution From Physical-Synthesis to GDSII



Achieve Highest Performance and Yield with Automation for RC Optimization and Design Reliability

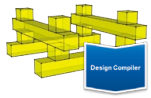
Via-Pillar Optimization Flow

Platform-Wide Convergent Implementation



N7 HPC Support in Design Compiler

Capacity and Performance for Largest HPC Designs



- Timing correlation
  - Accurate RC estimation across multiple layers
  - Estimation of Arnoldi effect for long nets
- Consistency checker to validate environment consistency between DCG and IC Compiler II
- Single command within DCG to forward required data to IC Compiler II
  - Netlist, floorplan, SDC, MCMM…

What-If Analysis

- Extraction and timing analysis for via pillars
- Support for incremental compile
- Output via-pillar guidance to IC Compiler II

Automated Performance Flow

- Automatic and manual EM-via inference / insertion
- Convergent performance-via flow through synthesis and implementation

N7 HPC Support in Design Compiler

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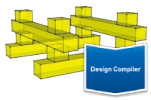

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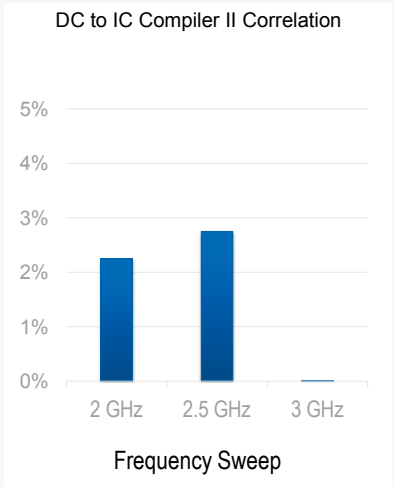
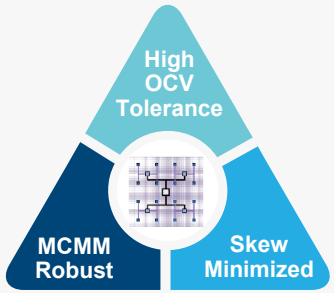


OCV-Tolerant Clock Construction

H-Tree as Structural Basis for Variation Minimization

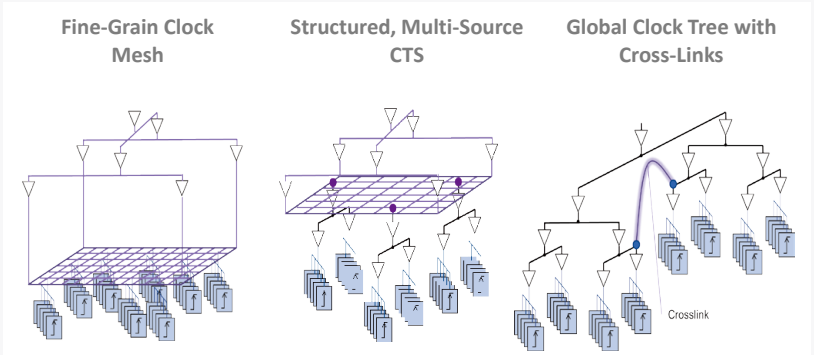
- High accuracy H-Tree Implementation using shape-based routing technology
  - Efficient load-balancing
  - Minimized route-resource usage
  - Reduced short-circuit power
- Optimized buffer selection and clock-area minimization
  - Natively Implements Via-Pillar flow
- Use in conjunction with other clock styles for QoR flexibility



Native Via-Pillar Support

Multiple Structured-CTS Solutions

Numerous Topologies for Proactive OCV Minimization



Unified UI Delivers Fast Trade-Off Analysis and Implementation

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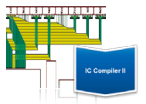
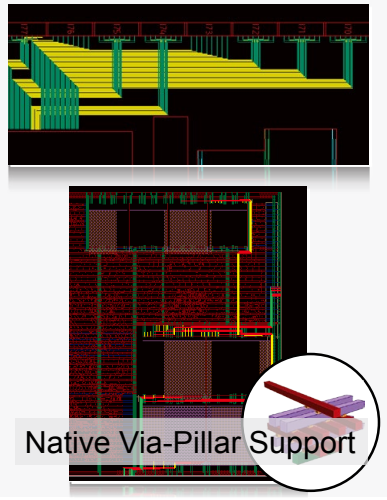
High-Performance Bus Routing

Shape-Based Router Delivers Targeted Performance



- Key Benefits
  - Routing of "server-class" busses
  - Route hundreds of buses simultaneously
  - Fully automated; no user guidance required
  - Support for user-defined topology control
- Define multiple bus constraints
  - Net group
  - Routing constraints: valid routing layer, NDR, topology control, shielding, etc



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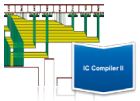
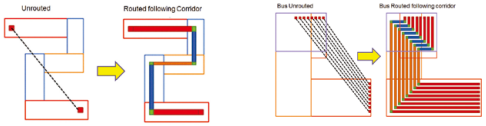
Example: DDR Busses



Any Route Topology



With High Accuracy Length Matching

Automation and Accuracy for Highest Performance Results

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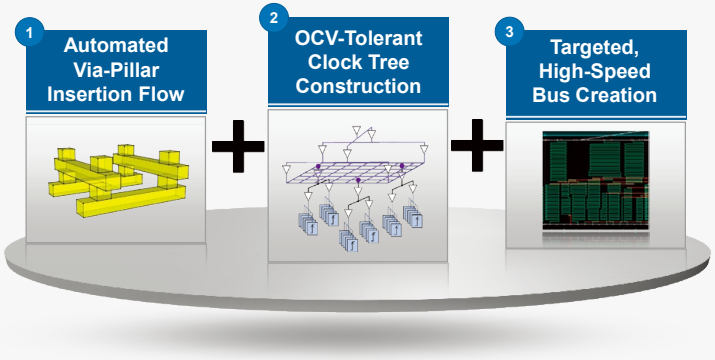
Synopsys' N7 HPC Design Flow

Full-Flow Solution Maximizing the Benefits of TSMC's Latest Node



Co-Optimized HPC Design Flow for Next Generation SoCs

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